AMENDMENTS

IN THE SPECIFICATION:

1. Please replace paragraph [0036] with the following amended paragraph:

[0036] In accordance with the present invention, the stable clock signal Z produced by ~~**the phase regulator**~~**clock signal counter 10** in the phase locked loop 6 (PLL) is used only as an intermediate signal "b." For the actual application 4 operated on the bus system 3 by the reception unit 2, another continuously present clock signal "a" is produced. This is done using a further clock transmitter 7' which produces second primary clock signals and a frequency divider 9' connected downstream. The output signals therefrom are applied to a clock signal counter 10' connected downstream. The way in which these components work is thus essentially equivalent to that for the phase locked loop 6.